查询L4903供应商

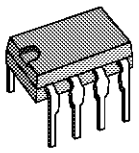
SGS-THOMSON MICROELECTRONICS

L4903

DUAL 5V REGULATOR WITH RESET AND DISABLE FUNCTIONS

PRELIMINARY DATA

- OUTPUT CURRENTS : I_{01} = 50mA
  I_{02} = 100mA
- FIXED PRECISION OUTPUT VOLTAGE 5V ± 2 %
- RESET FUNCTION CONTROLLED BY INPUT VOLTAGE AND OUTPUT 1 VOLTAGE
- RESET FUNCTION EXTERNALLY PROGRAMMABLE TIMING
- RESET OUTPUT LEVEL RELATED TO OUTPUT 2
- OUTPUT 2 INTERNALLY SWITCHED WITH ACTIVE DISCHARGING
- OUTPUT 2 DISABLE LOGICAL INPUT
- LOW LEAKAGE CURRENT, LESS THAN 1µA AT OUTPUT 1
- INPUT OVERVOLTAGE PROTECTION UP TO 60V
- RESET OUTPUT NORMALLY LOW
- OUTPUT TRANSISTORS SOA PROTECTION
- SHORT CIRCUIT AND THERMAL OVERLOAD PROTECTION



Minidip

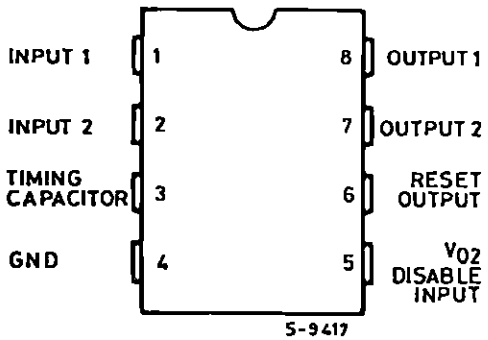
ORDERING NUMBERS : L4903

DESCRIPTION

The L4903 is a monolithic low drop dual 5 V regulator designed mainly for supplying microprocessor systems.

Reset, data save functions and remote switch on/off control can be realized.

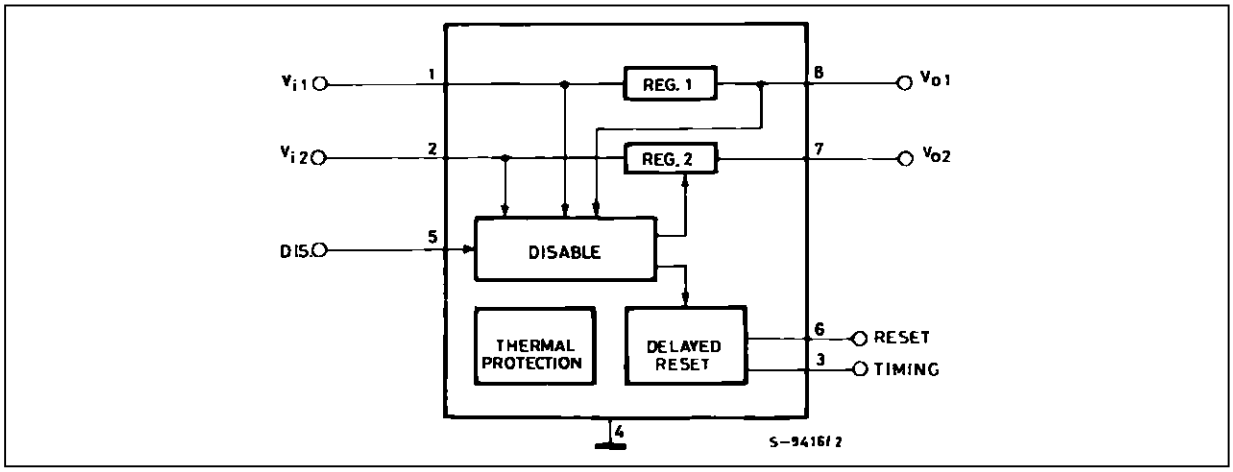
PIN CONNECTION



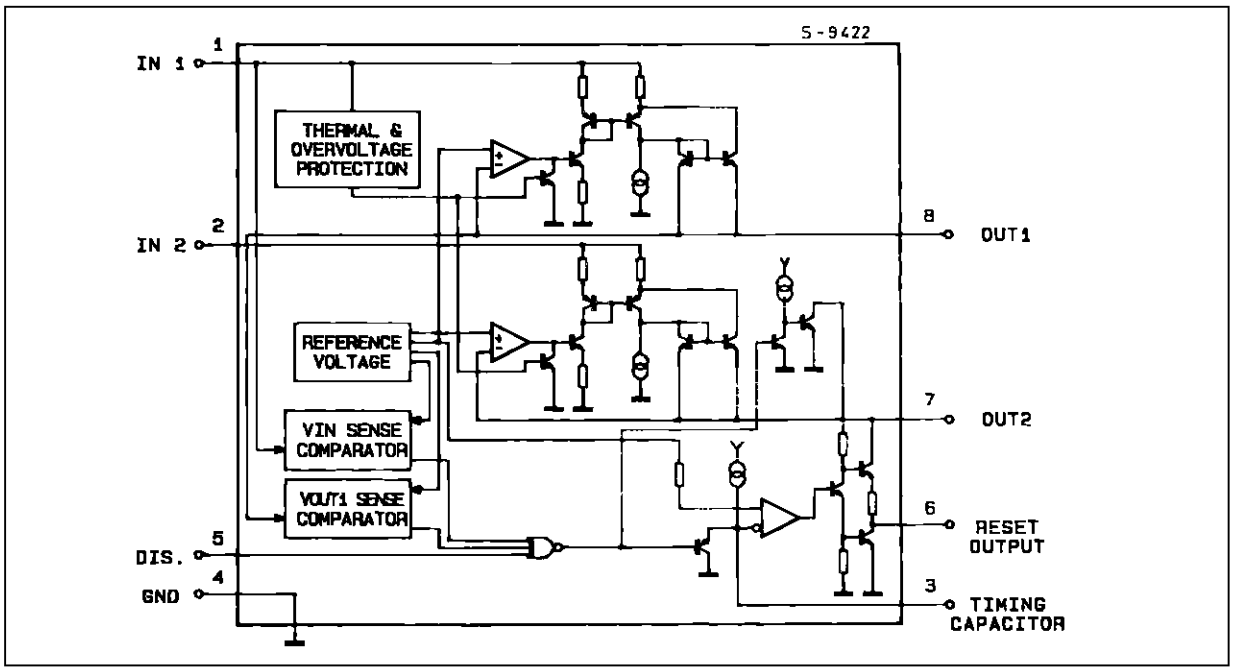
PIN FUNCTIONS

N°	Name	Function
1	Input 1	Low Quiescent Current 50mA Regulator Input
2	Input 2	100mA Regulator Input.
3	Timing Capacitor	If Reg. 2 is switched-ON the delay capacitor is charged with a 10µA constant current. When Reg. 2 is switched-OFF the delay capacitor is discharged.
4	GND	Common Ground
5	Disable Input	A high level (> V_{DT}) disables output Reg. 2.
6	Reset Output	When pin 3 reaches 5V the reset output is switched low. Therefore $t_{RD} = C_t (\frac{5V}{10\mu A})$; t_{RD} (ms) = C_t (nF).
7	Output 2	5V – 100mA Regulator Output. Enabled if V_o 1 > V_{RT}. DISABLE INPUT < V_{DT} and $V_{IN\,2}$ > V_{IT}. If Reg. 2 is switched-OFF the C_{02} capacitor is discharged.
8	Output 1	5V – 50mA regulator output with low leakage in switch-OFF condition.

BLOCK DIAGRAM



SCHEMATIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{IN}	DC Input Voltage	24	V
V_t	Transient Input Overvoltage (t = 40ms)	60	V
P_{tot}	Power Dissipation at T_{amb} = 50°C	1	W
T_{stg}, T_j	Storage and Junction Temperature	– 40 to 150	°C

THERMAL DATA

Symbol	Parameter		Value	Unit
$R_{th\ (j\text{-}pin)}$	Thermal Resistance Junction-pin 4	Max.	70	°C/W
$R_{th\ (j\text{-}a)}$	Thermal Resistance Junction-ambient	Max.	100	°C/W

ELECTRICAL CHARACTERISTICS (V_{IN} = 14.4V, T_{amb} = 25°C unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_i	DC Operating Input Voltage				20	V
V_{01}	Output Voltage 1	R Load 1kΩ	4.95	5.05	5.15	V
$V_{02\ H}$	Output Voltage 2 HIGH	R Load 1kΩ	V_{01} –0.1	5	V_{01}	V
$V_{02\ L}$	Output Voltage 2 LOW	I_{02} = – 5mA		0.1		V
I_{01}	Output Current 1 max. (*)	ΔV_{01} = – 100mV	50			mA
I_{L01}	Leakage Output 1 Current	V_{IN} = 0, $V_{01} \leq$ 3V			1	µA
I_{02}	Output Current 2 max. (*)	ΔV_{02} = – 100mV	100			mA
V_{I01}	Output 1 Dropout Voltage (*)	I_{01} = 10mA I_{01} = 50mA		0.7 0.75	0.8 0.9	V V
V_{IT}	Input Threshold Voltage		V_{01} + 1.2	6.4	V_{01} + 1.7	V
V_{ITH}	Input Threshold Voltage Hyst.			250		mV
ΔV_{01}	Line Regulation 1	7V < V_{IN} < 18V, I_{01} = 5mA		5	50	mV
ΔV_{02}	Line Regulation 2	7V < V_{IN} < 18V, I_{02} = 5mA		5	50	mV
ΔV_{01}	Load Regulation 1	V_{IN1} = 8V, 5mA < I_{01} < 50mA		5	20	mV
ΔV_{02}	Load Regulation 2	V_{IN1} = 8V, 5mA < I_{02} < 100mA		10	50	mV
IQ	Quiescent Current	$I_{01} = I_{02} \leq$ 5mA 0 < V_{IN} < 13V 7V < V_{IN} < 13V V_{02} LOW 7V < V_{IN} < 13V V_{02} HIGH		 4.5 2.7 1.6	 6.5 4.5 3.5	mA
I_{Q1}	Quiescent Current 1	6.3V < V_{IN1} < 13V, V_{IN2} = 0 $I_{01} \leq$ 5mA, I_{02} = 0		0.6	0.9	mA
V_{RT}	Reset Threshold Voltage		V_{02} – 0.04	4.7	V_{02} – 0.02	V
V_{RTH}	Reset Threshold Hysteresis		30	50	80	mV
V_{RH}	Reset Output Voltage HIGH	I_R = 500µA	V_{02} – 1	4.12	V_{02}	V
V_{RL}	Reset Output Voltage LOW	I_R = – 5mA		0.25	0.4	V
t_{RD}	Reset Pulse Delay	C_t = 10nF	3	5	11	ms
t_d	Timing Capacitor Discharge Time	C_t = 10nF			20	µs
V_{DT}	V_{02} Disable Threshold Voltage			1.25	2.4	V
I_D	V_{02} Disable Input Current	$V_D \leq$ 0.4V $V_D \geq$ 2.4V		- 150 30		µA µA
$\frac{\Delta V_{01}}{\Delta T}$, $\frac{\Delta V_{02}}{\Delta T}$	Thermal Drift	– 20°C ≤ T_{amb} ≤ 125°C		0.3 - 0.8		mV/°C
SVR1	Supply Voltage Rejection	f = 100Hz, V_R = 0.5V, Io = 50mA	50	84		dB
SVR2	Supply Voltage Rejection	f = 100Hz, V_R = 0.5V, I_o = 100mA	50	80		dB
T_{JSD}	Thermal Shut Down			150		°C

* The dropout voltage is defined as the difference between the input and the output voltage when the output voltage is lowered of 25 mV under constant output current condition.

TEST CIRCUIT

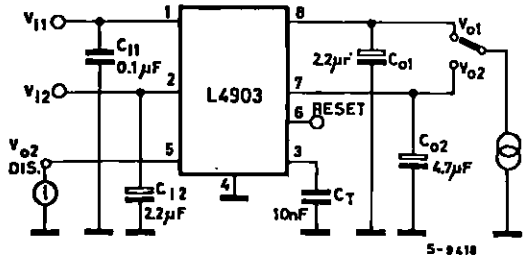
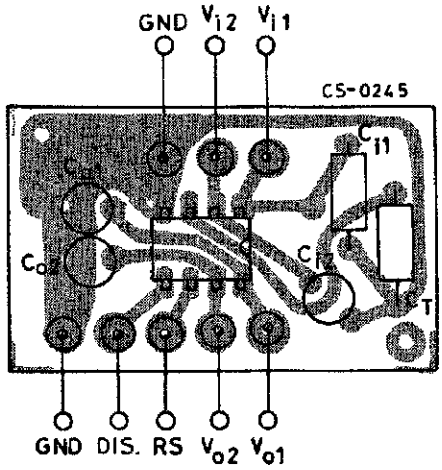


Figure 1 : P.C. Board and Components Layout of the Test Circuit



APPLICATION INFORMATION

In power supplies for µP systems it is necessary to provide power continuously to avoid loss of information in memories and in time of day clocks, or to save data when the primary supply is removed. The L4903 makes it very easy to supply such equipments ; it provides two voltage regulators (both 5 V high precision) with separate inputs plus a reset output for the data save function and Reg. 2 disable input.

CIRCUIT OPERATION (see Figure 2)

After switch on Reg. 1 saturates until V_{01} rises to the nominal value.

When the input 2 reaches V_{IT} and the output 1 is higher than V_{RT} the output 2 (V_{02} and V_R) switches on and the reset output (V_R) goes low after a programmable time T_{RD} (timing capacitor).

V_{02} is switched at low level and V_R at high level when one of the following conditions occurs ;
- a high level (> V_{DT}) is applied on pin 5 ;
- an input overvoltage ;
- an overload on the output 1 ($V_{01} < V_{RT}$) ;
- a switch off ($V_{IN} < V_{IT} - V_{ITH}$) ;

and they start again as before when the condition is removed.

An overload on output 2 does not switch Reg. 2, and does not influence Reg. 1.

The V_{01} output features :
- 5 V internal reference without voltage divider between the output and the error comparator
- very low drop series regulator element utilizing current mirrors

permit high output impedance and then very low leakage current even in power conditions.

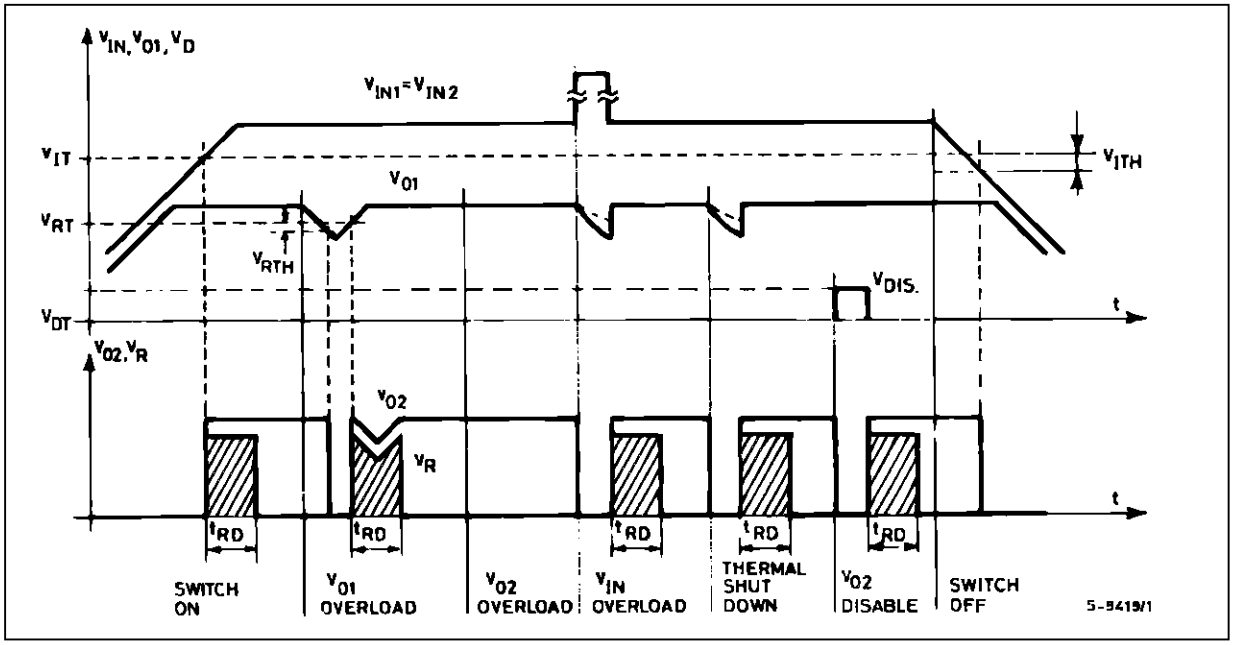
This output may therefore be used to supply circuits continuously, such as volatile RAMs, allowing the use of a back-up battery.

The V_{02} can supply other non essential 5 V circuits which may be powered down when the system is inactive, or that must be powered down to prevent uncorrect operation for supply voltages below the minimum value.

The reset output can be used as a "POWER DOWN INTERRUPT", permitting RAM access only in correct power conditions, or as a "BACK-UP ENABLE" to transfer data into in a NV SHADOW MEMORY when the supply is interrupted.

The disable function can be used for remote on/off control of circuits connected to the V_{02} output.

Figure 2



APPLICATION SUGGESTION

Figure 3 illustrates how the L4903's disable input may be used in a CMOS µComputer application. The V_{01} regulator (low consumption) supply permanently a CMOS time of day clock and a CMOS computer chip with volatile memory. V_{02} output, supplying non-essential circuits, is turned OFF under control of a µP unit.

Configurations of this type are used in products where the OFF switch is part of a keyboard scanned by a micro which operates continuously even in the OFF state.

Figure 3

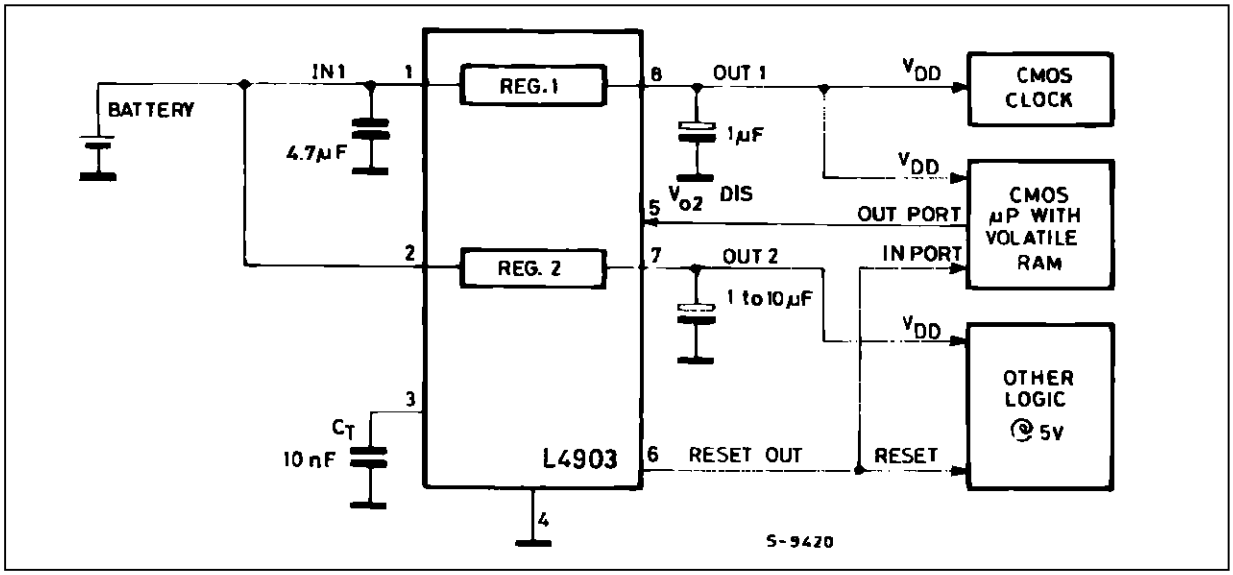


Figure 4 : Quiescent Current (reg. 1) versus Output Current

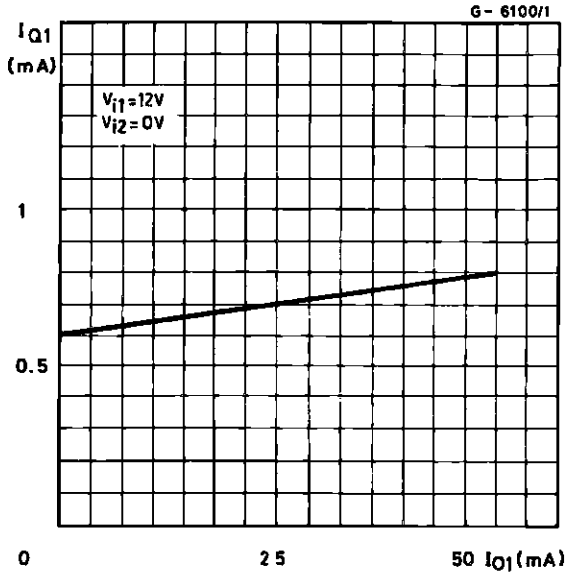


Figure 5 : Quiescent Current (reg. 1 versus Input Voltage

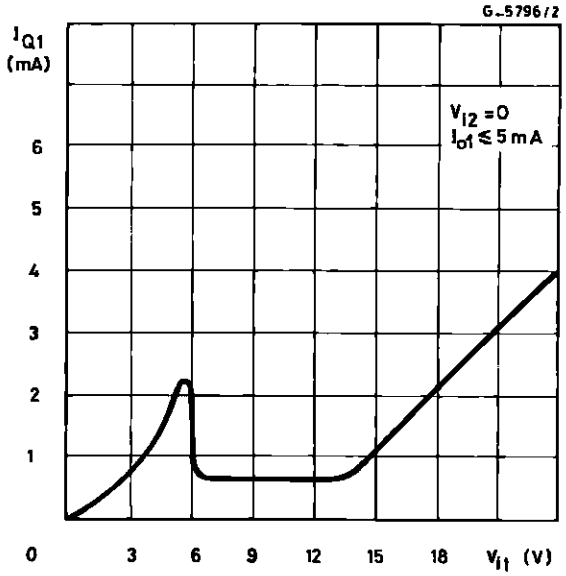


Figure 6 : Total Quiescent Current versus Input Voltage

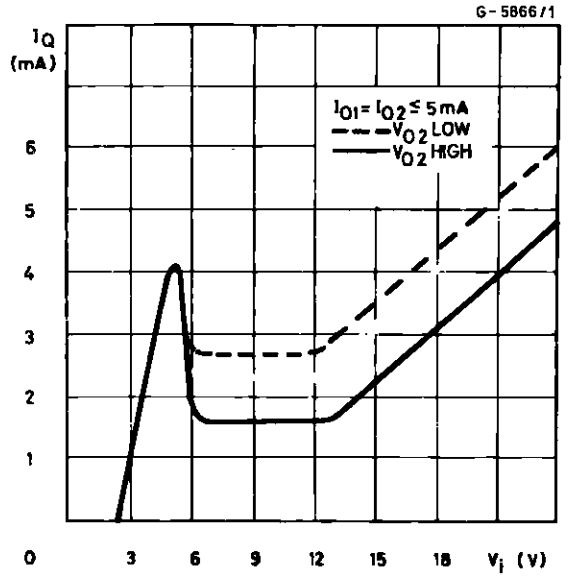
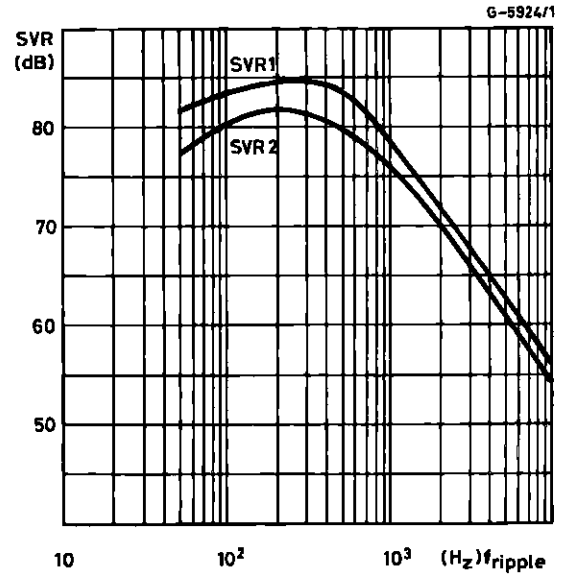
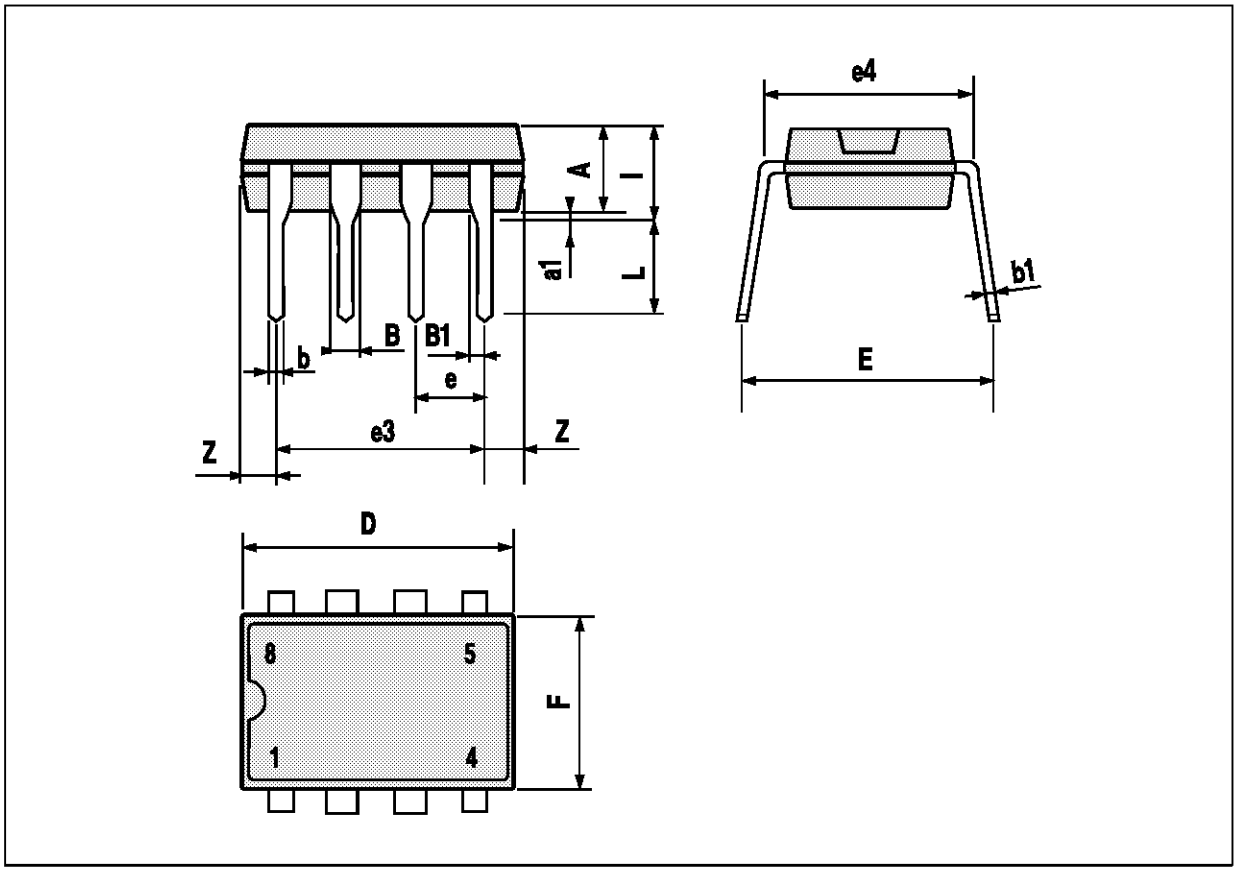


Figure 7 : Supply Voltage Rejection Regulators 1 and 2 versus Input Ripple Frequence



MINIDIP PACKAGE MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A		3.32			0.131	
a1	0.51			0.020		
B	1.15		1.65	0.045		0.065
b	0.356		0.55	0.014		0.022
b1	0.204		0.304	0.008		0.012
D			10.92			0.430
E	7.95		9.75	0.313		0.384
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			6.6			0.260
I			5.08			0.200
L	3.18		3.81	0.125		0.150
Z			1.52			0.060



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